REMARKS

A certified copy of the Korean Patent Application No. 2000-61478 from which the current application claims priority is provided herewith.

The Examiner has objected to the specification, stating that the recitations "to y switch" and the recitation "baseband analog ASIC (BBA)" are ambiguous. Accordingly, the specification has been amended to overcome the Examiner's stated objections.

The Examiner has objected to Claims 1, 4 and 6 because of the use of the recitation "to for" in Line 3 of Claim 1, the use of the recitation "the radio receiver for the transmission burst period" in Line 5 of Claim 4, and the use of the recitation "the radio receiver for the transmission burst period" in Line 5 of Claim 6. Accordingly, Claims 1, 4 and 6 have been amended to overcome the Examiner's stated objections.

Claims 1-6 are pending in this application. In the Office Action, the Examiner has rejected the Claims 1-6 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,185,411 B1 (Gillig).

Regarding the Examiner's rejection of independent Claim 1 under 35 U.S.C. §102(e), the Examiner states that Gillig teaches all the recitations of Claim 1. Upon review of the cited references, it is respectfully submitted that the Examiner is incorrect. Gillig teaches an apparatus and method which enables elements of a phase locked loop (PLL). Gillig further teaches "[t]he controller 301 enables a first element of the plurality of elements, having a first response time, at the first time responsive to the first control signal at line 302, and enables a second element of the plurality of elements, having a second response time less than the first response time, responsive to the first response time and the second control signal." (Column 4, Lines 38-46, and FIGs. 3-5). Gillig further teaches "the first element of the plurality of

Lines 38-46, and FIGs. 3-5). Gillig further teaches "the first element of the plurality of elements is a voltage controlled oscillator," "the second element of the plurality of elements is a loop divider" (Column 4, Lines 48-52), and that "[c]ontrol signal 303 *keeps the other elements of the PLL 300 disabled.*" (Column 5, Lines 36-37, emphasis added). In other words, Gillig teaches a PLL wherein only select elements of the PLL are enabled and that other elements of the PLL are disabled (for example, the phase detector 202 is not enabled and does not produce a phase error signal at line 207 during warm-up of the PLL so that the PLL can lock in less time than was known. Contrary to that which is taught by Gillig, Claim 1 recites "a controller configured to control the first PLL block to operate *before a minimum time period* required for the first PLL block to lock up from the start point of a transmission burst period, and to control the second PLL block to operate *before a minimum time period* required for the second PLL block to lock up from the start point of a reception burst period"(emphasis added), which is not taught by Gillig. Accordingly, it is believed that the Examiner's rejection of Claim 1 is improper and therefore should be withdrawn.

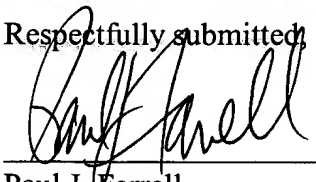
Regarding the Examiner's rejection of independent Claims 2-3 and 5 under 35 U.S.C. §102(e), it is respectfully submitted that the Examiner is incorrect. As discussed above, Gillig teaches an apparatus and method that enables elements of a phase locked loop (PLL) wherein only select elements of the PLL are activated and that other elements of the PLL are deactivated during warm-up of the PLL so that the PLL can lock in less time than was known. Gillig does not teach "a controller for controlling the first PLL block to operate *before an end point of a reception burst period* and controlling the second PLL block to operate *before an end point of a transmission burst period*" (emphasis added) as recited in Claim 2. Furthermore, Gillig does not teach "controlling the first PLL block to operate *before a minimum time period required for*

the first PLL block to lock up from the start point of a transmission burst period; and controlling the second PLL block to operate *before a minimum time period required for the second PLL block to lock up* from the start point of a reception burst period" (emphasis added) as recited in Claim 3. Moreover, Gillig does not teach "controlling the first PLL block to operate *before the end point of a reception burst period*; and controlling the second PLL block to operate *before the end point of a transmission burst period*" (emphasis added) as recited in Claim 5. Accordingly, it is believed that the Examiner's rejection of independent Claims 2, 3 and 5 under 35 U.S.C. §102(e), is improper and therefore should be withdrawn.

In light of the discussion above, it is respectfully submitted that independent Claims 1-3 and 5 overcome the stated rejections. Without conceding the patentability per se of dependent Claims 4 and 6 it is respectfully submitted that these claims also overcome the rejections by virtue of their dependence on Claims 3 and 5, respectively. Claims 1-6 are believed to be in condition for allowance.

Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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